

WHAT IS CLAIMED IS:

- 1 1. A method for making a semiconductor package comprising:
2 (a) molding a molding material around a leadframe structure
3 having a die attach region and a plurality of leads, wherein the die attach region is
4 exposed through a window in the molding material; and
5 (b) after (a), mounting a semiconductor die to the die attach region
6 using a flip chip mounting process.
- 1 2. The method of claim 1 wherein the semiconductor die
2 comprises a vertical power MOSFET.
- 1 3. The method of claim 1 wherein the plurality of leads include at
2 least one source lead and at least one gate lead.
- 1 4. The method of claim 1 further comprising, after (b):
2 reflowing solder that is between the die attach region of the leadframe
3 and the semiconductor die.
- 1 5. The method of claim 1 wherein the die attach region comprises
2 at least one aperture.
- 1 6. The method of claim 1 wherein molding comprises placing the
2 leadframe structure in a molding tool.
- 1 7. The method of claim 1 further comprising depositing solder on
2 the die attach region of the leadframe structure and within the window.
- 1 8. The method of claim 1 wherein the plurality of leads comprises
2 a source lead and a gate lead.
- 1 9. The method of claim 1 further comprising:
2 attaching a heat plate structure to the leadframe structure.

10. A semiconductor package comprising:
 - (a) a leadframe structure comprising a die attach region and plurality of leads;
 - (b) a molding material molded around at least a portion of the leadframe structure, and wherein the molding material comprises a window; and
 - (c) a semiconductor die comprising an edge mounted on the die attach region, wherein the semiconductor die is within the window, and wherein a gap is present between the edge of the semiconductor die and the molding material.
11. The semiconductor package of claim 10 wherein the leadframe structure comprises copper.
12. The semiconductor package of claim 10 wherein the semiconductor die comprises a vertical power transistor including a source region, a gate region, and a drain region, wherein the source region and the gate region are proximate the die attach region and the drain region is distal to the die attach region.
13. The semiconductor package of claim 10 wherein the semiconductor package comprises bump and solder joints between the semiconductor die and the leadframe structure.
14. The semiconductor package of claim 10 wherein the window has dimensions that are greater than lateral dimensions of the semiconductor die.
15. The semiconductor package of claim 10 wherein the molding material comprises an epoxy molding material.
16. The semiconductor package of claim 10 wherein the window is a first window and wherein the molding material comprises a second window, the second window exposing a surface of the leadframe structure opposite to the die attach region.
17. The semiconductor package of claim 16 further comprising a heat sink coupled to the leadframe structure through the second window.

18. The semiconductor package of claim 10 further comprising an array of joints coupling the semiconductor die and the leadframe structure, wherein the array of joints comprises a solder or non-solder bump material and a solder paste material including different melting temperatures.

19. An electrical assembly comprising:
a semiconductor package comprising (a) a leadframe structure comprising a die attach region and plurality of leads, (b) a molding material molded around at least a portion of the leadframe structure and wherein the molding material comprises a window, and (c) a semiconductor die comprising an edge mounted on the die attach region, wherein the semiconductor die is within the window, and wherein a gap is present between the edge and the molding material; and
a circuit substrate, wherein the semiconductor package is mounted to the circuit substrate.

20. The electrical assembly of claim 19 further comprising solder coupling the semiconductor die.